The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board

---

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte DONALD EUGENE DENNING, ROBERT GEORGE EMBERTY, and CRAIG ANTHONY KLEIN

Appeal No. 2006-1656
Application 09/131,846[1]

ON BRIEF

Before BARRETT, LEE, and LEVY, *Administrative Patent Judges.*

BARRETT, *Administrative Patent Judge.*

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1-19.

We reverse.

PREVIOUS BOARD DECISION

A previous decision was entered in Appeal No. 2002-1859 on June 30, 2004.

---

[1] Application for patent filed July 24, 1998, entitled "Data Processing Method and System for Simulation of Hardware Faults Utilizing a PCI Bus."

BACKGROUND

The invention relates to a method and system in a data processing system for simulating a hardware fault for a peripheral component interconnect (PCI) bus.

Claim 1 is reproduced below, where the underlined words indicate additions to claim 1 considered in the previous appeal.

> 1. A method in a data processing system for simulating a hardware fault occurring on an expansion card, said expansion card coupled to a processing unit in said system utilizing a bus, said method comprising the steps of:
>
> specifying said hardware fault to simulate;
>
> determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card;
>
> creating an analog voltage signal representative of said specified hardware fault <u>utilizing a digital-to-analog converter</u>; and
>
> outputting said analog voltage signal during operation of said expansion card, wherein said hardware fault occurring on said expansion card is simulated.

THE REFERENCES

The examiner relies on the following references:

Gates	5,701,409	December 23, 1997

PCI Local Bus Specification, Chapter 4, Revision 2.2, December 18, 1998.

THE REJECTION

Claims 1-19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Gates. The PCI specification is relied upon in addressing appellants' arguments. The examiner finds that "the digital-to-analog converter as described by Applicant is inherent to the PCI specification" (final rejection, page 3) and "Gates clearly provides for this DAC functionality, taking a digital signal and conditioning it through analog manipulation for transport on the PCI bus with vary [sic, very] different physical requirements than that of the board from which the original digital signal was received" (final rejection, page 6). The examiner cites the PCI specification as evidence that the bus interface specifies the characteristics of the analog voltage signal inputs.

We refer to the final rejection entered March 8, 2005, and the examiner's answer (pages referred to as "EA__") entered September 16, 2005, for a statement of the examiner's rejection, and to the appeal brief (pages referred to as "Br__") received August 5, 2005, for a statement of appellants' arguments thereagainst.

DISCUSSION

Gates discloses an integrated circuit with a built-in bus error generation circuit for simulating a hardware fault on a PCI bus. During test, an error command (Fig. 7) is loaded into a command register of the bus error generation circuit via the bus terminals (abstract; col. 6, lines 10-20 & 60-64). The bus error generation circuit then decodes the command and either generates or simulates an error condition on the bus during a subsequent bus cycle (abstract). Status configuration registers are then read to determine whether the integrated circuit and other

devices properly detected and/or handled the generated or simulated error (abstract; summary). The generated and simulated error condition commands cause incorrect parity values to be output onto the parity bus terminal to simulate one of several different error conditions on the PCI bus (e.g., col. 4, lines 32-42), such as a "Master Address Parity Error" (MADRSPARERR), "Master Write Data Parity Error" (MWDATAPARERR), or a "Target Data Parity Error" (TRDATAPARRERR). Generating a parity error requires changing only the value of digital data on the bus.

Appellants refer to the statement in our previous opinion at pages 5-6: "It seems to us that appellants' invention may be the use of a DAC to generate the voltage signal representative of a hardware fault, as opposed to the use of logic gates (such as XOR gate 109 in Fig. 3) in Gates. However, the examiner correctly noted that a DAC is not claimed. If it was, the examiner would then have tried to find prior art to show the obviousness of using a DAC in place of a logic gate." Appellants note that the claims were amended to expressly recite a digital-to-analog (DAC) converter (Br4), but that the examiner dismisses this statement in finding a digital-to-analog converter to be inherent (Br5). Appellants argue that nothing in the PCI specification refers to the utilization of a digital-to-analog converter and dispute the examiner's finding that this element is "inherent" within the PCI specification. "In support of this position Applicant urges the Board to consider that if the utilization of a digital-to-analog converter is inherent then why does *Gates* teach the utilization of an XOR gate having a digital output, as depicted at element 109 of Fig. 3 of *Gates*?" (Br5.)

The examiner states (EA7):

> The Examiner believes that the PCI interface inherent to Gates performs the claimed functionality of the "digital-to-analog voltage converter." Column 4, line 1 of Gates states "Integrated circuit 100 includes a plurality of bus interface terminals 103-107 and a bus error generation circuit. . ." Interface terminals are used when transferring data from one analog domain in which digital data processing occurs to a different analog domain in which transmission occurs, for instance from a high speed, low noise silicon-based field effect transistor network to slower speed, high noise copper-based PCI bus. Gates mentions, in passing, the use of a PCI interface to carry out this operation, as to one of ordinary skill in the [art] does not need a complete and thorough explanation of how interfaces work (column 4, lines 11-31).
>
> The Examiner points out, Applicant's own specification assigns this functionality to the DAC, the associated relays and the associated buffers at pages 7, line 26 through page 8, line 4. The PCI specification provides a very rigorous set of parameters for how the analog voltage signals representing data may be constructed (Chapter 4, of the PCI specification discusses these parameters). Applicant does not claim or disclose the structure or manner of internal operation of the "digital-to-analog voltage converter." This makes the PCI interface and "digital-to-analog voltage converter" functionally equivalent in the claims. Thus the Examiner believes PCI interface as taught by Gates carries out the claimed limitation of "creating an analog voltage signal representative of said specified hardware fault."

In response to the argument that the XOR gate 109 has a digital output, the examiner responds that this output is actually the digital input to the PCI interface that functions as the claimed digital-to-analog converter (EA8). The examiner distinguishes between a "digital-to-analog converter" and a "digital-to-analog voltage converter." A "digital-to-analog converter" is interpreted to be an element "used to take [a digital] number and output an analog signal" (EA8), whereas a "'digital-to-analog voltage converter' is used to condition digital data with one set of analog properties for unsuitable [sic, unsuitable for] transmission to the same digital data with a different set of analog properties suitable for transmission, for instance taking the digital

video signal from co-axial cable line and transforming the digital signal's analog properties to allow processing by the digital cable set top box" (EA8-9).

We disagree with the examiner's interpretation of "digital-to-analog voltage converter" as a device to convert a digital signal with one set of analog properties to a digital signal with a different set of analog properties. While we understand that the examiner is trying to interpret the claims as broadly as possible, the examiner has not cited any support for this interpretation and the interpretation is considered unreasonable. We interpret "digital-to-analog voltage converter" to mean a device that converts a "digital" number "to" an "analog voltage"; the claims specifically recite that the "digital-to-analog voltage converter" creates an analog voltage signal. It is clear that a "digital-to-analog converter" requires a digital input and an analog output. The addition of the word "voltage" qualifies the output as a voltage; DAC converters can have current or voltage outputs. A "digital-to-analog converter" implies that the digital input is at least two bits because a single bit would simply be a digital system. The examiner focuses on the "analog voltage converter" part of "digital-to-analog voltage converter" and ignores the "digital" part of the conversion. The examiner essentially interprets "digital-to-analog voltage converter" to be an "analog-to-analog voltage converter."

Gates does not convert a digital signal to an analog voltage, expressly or inherently. We stated in our previous decision that digital signals (logical 0s and 1s) are represented as analog voltages with certain predetermined ranges, and that the digital signal in Gates was broadly "an analog voltage signal." However, finding that a digital signal is represented as an analog voltage

is not the same as saying that a digital signal is converted to an analog voltage. "Digital-to-analog voltage conversion" requires converting a binary number to an analog value corresponding to that binary number, which simply is not done in Gates. Gates is strictly a digital circuit because the values on the PCI bus are digital. The PCI interface may condition the analog voltages by converting one analog voltage representing a digital value to another analog voltage representing the same digital value, but this is at best an analog-to-analog conversion.

Claim 1 recites a "method in a data processing system" including the step of "creating an analog voltage signal representative of said specified hardware fault utilizing a digital-to-analog converter." Thus, claim 1 recites a method step in a system performed by a specific piece of hardware. The "digital-to-analog voltage converter" structure performs the function of converting digital numbers to analog voltages, which structure and function is not found in Gates. The anticipation rejection of claims 1-9 is reversed.

Claim 10 recites a "data processing system" including "a digital-to-analog voltage converter for creating an analog voltage signal representative of said specified hardware fault." The "digital-to-analog voltage converter" is a specific piece of hardware that performs the function of converting digital numbers to analog voltages, which structure and function is not found in Gates. The anticipation rejection of claims 10-19 is reversed.

CONCLUSION

The rejection of claims 1-19 is reversed.

REVERSED

LEE E. BARRETT
Administrative Patent Judge

JAMESON LEE
Administrative Patent Judge

STUART S. LEVY
Administrative Patent Judge

BOARD OF PATENT
APPEALS
AND
INTERFERENCES

DILLON & YUDELL LLP
8911 NORTH CAPITAL OF TEXAS HWY
SUITE 2110
AUSTIN, TX 78759